



# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 684.3067

First Named Inventor or Application Identifier

ICHIRO TANAKA

Express Mail Label No.

## APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

## ADDRESS TO:

Commissioner for Patents  
Box Patent Application  
Washington, DC 20231

1. ☐ Fee Transmittal Form  
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification Total Pages 28

3. ☒ Drawing(s) (35 USC 113) Total Sheets 15

4. ☒ Patent Application Bibliographic  
Data Sheet Total Sheets 1

5. ☐ Oath or Declaration Total Pages

- a. ☐ Newly executed (original or copy)  
b. ☐ Unexecuted for information purposes  
c. ☐ Copy from a prior application (37 CFR 1.63(d))  
(for continuation/divisional with Box 18 completed)  
[Note Box 6 below]

i. ☐ DELETION OF INVENTOR(S)  
Signed Statement attached deleting inventor(s)  
named in the prior application, see 37 CFR  
1.63(d)(2) and 1.33(b).

6. ☐ Incorporation By Reference (useable if Box 5c is checked)  
The entire disclosure of the prior application, from which a copy of the  
oath or declaration is supplied under Box 5c, is considered as being  
part of the disclosure of the accompanying application and is hereby  
incorporated by reference therein. The incorporation can only be  
relied upon when a portion has been inadvertently omitted from the  
submitted application parts.

7. ☐ Microfiche Computer Program (Appendix)

8. ☐ Nucleotide and/or Amino Acid Sequence Submission  
(if applicable, all necessary)

a. ☐ Computer Readable Copy

b. ☐ Paper Copy (identical to computer copy)

c. ☐ Statement verifying identity of above copies

## ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))

10. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney  
(when there is an assignee)

11. ☐ English Translation Document (if applicable)

12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS  
Citations

13. ☒ Preliminary Amendment

14. ☒ Return Receipt Postcard (MPEP 503)  
(Should be specifically itemized)

15. ☐ Small Entity Statement(s) ☐ Statement filed in prior application  
Status still proper and desired

16. ☐ Certified Copy of Priority Document(s)  
(if foreign priority is claimed)

17. ☐ Other: \_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

18. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No. \_\_\_\_/\_\_\_\_\_  
Prior application information: Examiner \_\_\_\_\_ Group/Art Unit: \_\_\_\_\_

## 19. CORRESPONDENCE ADDRESS

☒ Customer Number or Bar Code Label

05514

(Insert Customer No. or Attach bar code label here)

or ☐ Correspondence address below

NAME

Address

City

State

Zip Code

Country

Telephone

Fax



CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	25-20 =	5	X \$ 18.00 =	\$ 90.00
	INDEPENDENT CLAIMS (37 CFR 1.16(b))	3-3 =	0	X \$ 78.00 =	\$ 0.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			\$260.00 =	\$ 260.00
				BASIC FEE (37 CFR 1.16(a))	\$ 690.00
			Total of above Calculations =		\$1040.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				
	TOTAL =				\$1040.00

20. Small entity status

- a. ☐ A small entity statement is enclosed
- b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
- c. ☐ Is no longer claimed.

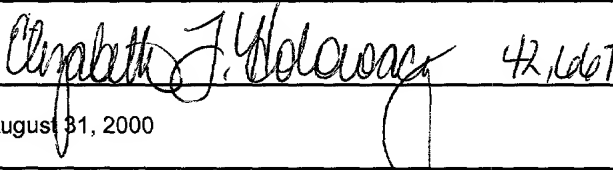
21. ☒ A check in the amount of \$ 1040.00 to cover the filing fee is enclosed.

22. ☐ A check in the amount of \$ \_\_\_\_\_ to cover the recordal fee is enclosed.

23. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:

- a. ☒ Fees required under 37 CFR 1.16.
- b. ☒ Fees required under 37 CFR 1.17.
- c. ☐ Fees required under 37 CFR 1.18.

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED**

NAME	Elizabeth F. Holowacz
SIGNATURE	 42,1667
DATE	August 31, 2000

Variable	Mean	SD	Min	Max
Age	38.5	10.5	25	55
Gender	0.5	0.5	0	1
Marital status	0.5	0.5	0	1
Education	12.5	1.5	10	15
Income	1.5	0.5	1	2
Health status	1.5	0.5	1	2
Stress level	1.5	0.5	1	2
Life satisfaction	1.5	0.5	1	2
Work satisfaction	1.5	0.5	1	2
Family satisfaction	1.5	0.5	1	2
Community satisfaction	1.5	0.5	1	2
Overall satisfaction	1.5	0.5	1	2
Life expectancy	75	5	65	85
Health expectancy	65	5	55	75
Quality of life	1.5	0.5	1	2
Life expectancy (years)	75	5	65	85
Health expectancy (years)	65	5	55	75
Quality of life (score)	1.5	0.5	1	2
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Quality of life (score)	1.5	0.5	1	2
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Health expectancy (years)	65	5	55	75
Quality of life (score)	1.5	0.5	1	2
Life expectancy (years)	75	5	65	85
Health expectancy (years)	65	5	55	75
Quality of life (score)	1.5	0.5	1	2
Life expectancy (years)	75	5	65	85
Health expectancy (years)	65	5	55	75
Quality of life (score)	1.5	0.5	1	2
Life expectancy (years)	75	5	65	85
Health expectancy (years)	65	5	55	75
Quality of life (score)	1.5	0.5	1	2
Life expectancy (years)	75	5	65	85
Health expectancy (years)	65	5	55	75
Quality of life (score)	1.5			

CORRESPONDENCE INFORMATION

APPLICATION INFORMATION

Total Drawing Sheets:: 15  
Formal Drawings?: Yes  
Application Type:: Utility  
Docket Number:: 684.3067  
Secrecy Order in Parent Appl.?: No

Representative Customer Number:: 5514

Foreign Application One:: 250853/1999  
Filing Date:: 09-03-1999  
Country:: Yes  
Priority Claimed:: Yes

684.3067

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: )  
: Examiner: Unassigned  
ICHIRO TANAKA )  
: Group Art Unit: Unassigned  
Application Based on )  
JP 250853/1999 :  
: )  
Filed: Herewith :  
: )  
For: TWO-DIMENSIONAL PHASE :  
ELEMENT AND METHOD OF )  
MANUFACTURING THE SAME : August 31, 2000

Commissioner for Patents  
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits of the above-identified application, please amend the application as follows.

In the Claims:

Please amend claims 2-4, 6-13 and 15 as follows:

2. (Amended) A method of manufacturing a two-dimensional phase type element[, ] comprising the steps of:  
forming[, on a substrate,] a first etching mask in a checkered pattern on a substrate; and

performing an etching process [while] using the mask as a reference.

3. (Amended) A method of manufacturing a two-dimensional phase type element[, ] comprising the steps of:

forming[, on a substrate,] a first etching mask in a checkered pattern on a substrate;

forming segments of multiple levels at a portion not covered by the first etching mask;

forming a second etching mask corresponding to an inversion of the first etching mask;

removing the first etching mask; and

forming segments of multiple levels at a portion not covered by the second etching mask.

4. (Amended) A method according to Claim 2 or 3, wherein the first etching mask [is formed by a] consists of chromium [film].

6. (Amended) A method according to Claim [2 or] 3, wherein the first etching mask consists of aluminum and wherein the second etching mask consists of chromium.

7. (Amended) A method according to Claim [2 or] 3, wherein the first etching mask consists of chromium and wherein the second etching mask consists of aluminum.

8. (Amended) A method according to [any one of Claims 2-7] Claim 2 or 3, wherein the substrate contains quartz.

9. (Amended) A method according to [any one of Claims 2-8] Claim 2 or 3, wherein a reticle having an optical proximity effect correcting pattern is used to form the etching mask [of] having a checkered pattern through photolithography.

10. (Amended) A method according to [any one of Claims 2-9] Claim 2 or 3, wherein the etching process is carried out by use of the etching mask and an etching mask formed by a resist.

11. (Amended) A method according to [any one of Claims 2-10] Claim 2 or 3, further comprising the step of:  
molding an element while using, as a mold, a substrate on which plural segments of multiple levels are formed.

12. (Amended) A method according to [any one of Claims 2-11] Claim 2 or 3, wherein the method is usable to produce one of a phase type computer generated hologram, a two-dimensional binary structure, and a phase modulation plate.

13. (Amended) An illumination system including a two-dimensional phase type element manufactured in accordance with a method as recited in [any one of Claims 2-12] Claim 2 or 3.

15. (Amended) A device manufacturing method[,]  
comprising the steps of:

exposing a wafer to a device pattern[, by use of]  
using a projection exposure apparatus as recited in Claim 14;  
and

developing the exposed wafer.

#### Remarks

The claims are 1-15, with claims 1-3 being independent. Claims 2-4, 6-13 and 15 have been amended to better define the invention. In particular, claims 8-13 have been amended to remove improper multiple dependency. Claims 2-4, 6, 7 and 15 have been amended as to formal matters. Consideration of the claims is respectfully requested.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All

correspondence should continue to be directed to our below  
listed address.

Respectfully submitted,

  
Attorney for Applicant

Registration No. 42,667

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TWO-DIMENSIONAL PHASE ELEMENT AND  
METHOD OF MANUFACTURING THE SAME

FIELD OF THE INVENTION AND RELATED ART

5           This invention relates to a two-dimensional  
phase element such as a phase type computer generated  
hologram (CGH), a two-dimensional binary structure or  
a phase modulation plate, for example, usable as an  
optical component of a semiconductor manufacturing  
10 reduction exposure apparatus or a component of an  
optical interconnection element, for example. In  
another aspect, the invention concerns a method of  
manufacturing a mold for such two-dimensional element.

15           A paper "O plus E" No.11, pp95-100 (1996)  
discloses a method of manufacturing a step-like shape  
on a substrate, through repetition of resist  
application, resist mask patterning and etching. If  
the number of masks is L, a multiple level phase type  
CGH having a phase level of  $2^L$  is obtainable.

20           Figures 24A - 24C are plan views of reticles  
to be used for photolithography, in the manufacture of  
a phase type CGH. More specifically, Figures 24A, 24B  
and 24C show patterns of reticles 1a, 1b and 1c,  
respectively. Zones depicted by hatching are light  
25 blocking regions. The reticle 1a is used to perform  
an etching to a depth 61 nm. The reticle 1b is used  
to perform an etching to a depth 122 nm. The reticle

1c is used to perform an etching to a depth 244 nm.  
These reticles 1a, 1b and 1c may be used in any order.  
However, a higher resist patterning precision is  
attainable if the etching is started in an order from  
5 a smaller etching-depth reticle, that is, the reticle  
1a.

First, a resist material is applied to a  
substrate, and the resist is then patterned by using  
the reticle 1a shown in Figure 24A. The thus produced  
10 resist pattern is then used as a mask, and an etching  
process is carried out to a depth 61 nm. The result  
is an etching depth distribution such as shown in  
Figure 25A. Numerals in the drawing denote the  
etching depth (nm). Thereafter, the resist pattern is  
15 separated, and a resist is again applied to the  
substrate. Then, the resist patterning is carried out  
by using the reticle 1b shown in Figure 24B. The thus  
produced resist pattern is used as a mask, and an  
etching process is carried out to a depth 122 nm,  
20 whereby an etching depth distribution such as shown in  
Figure 25B is produced. Subsequently, the resist  
pattern is separated, and a resist is applied again to  
the substrate. The resist is then patterned by using  
the reticle 1c shown in Figure 24C. The thus produced  
25 resist pattern is used as a mask, and an etching  
process is carried out to a depth 244 nm, whereby an  
etching depth distribution such as shown in Figure 25C

is produced.

In the photolithographic procedure described above, alignment of reticles is necessary. For manufacture of a multiple level phase type CGH, idealistically a shape such as shown in Figure 26 should be formed. Practically, however, there occurs an alignment error which causes an unwanted error at the edge of the shape, as shown in the sectional view of Figure 27.

Figure 28 is a plan view of a segment in a case where, due to an alignment error, a second-time resist pattern of a size "a" at each side is deviated in X direction by a length "d". Zones 11 depict the boundaries of segments defined by a first-time resist pattern. Zone 12 depicted by a thick solid line denotes the second-time resist pattern. Thus, zones 13 depicted by hatching are invalid regions as a phase type CGH, and the area  $S_1$  of the invalid regions can be given by:

$$S_1 = 2ad \quad \dots(1)$$

Figure 29 is a plan view of a segment in a case where, due to an alignment error, a second-time resist pattern is deviated in X and Y directions by a length "d". Zones 11 defined by narrow lines depict the boundaries of segments defined by a first-time resist pattern. Zone 14 depicted by a thick line denotes the second-time resist pattern. Thus, zones

15 depicted with hatching are invalid regions as a phase type CGH. The area  $S_2$  thereof can be given by:

$$S_2 = 4ad - 2d^2 \quad \dots(2)$$

On the other hand, where a phase type CGH  
5 manufactured in accordance with the method described above is incorporated into an illumination system, since the phase type CGH has invalid regions, light may be projected to an undesired position or the quality of an image formed by the phase type CGH may  
10 be deteriorated. Therefore, a desired performance may not be accomplished.

Where such an illumination system is incorporated into a projection exposure apparatus, a desired performance may of course be unattainable.

15 Also, where a semiconductor device is manufactured by use of such a projection exposure apparatus, the yield rate may be lowered and the device productivity may be slowed down. It may cause an increased device price.

#### 20 SUMMARY OF THE INVENTION

It is accordingly an object of the present invention to provide a two-dimensional phase type element and a method of manufacturing the same, by which a desired performance can be accomplished  
25 stably.

In accordance with an aspect of the present invention, there is provided a two-dimensional phase

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type element having plural segments, wherein an alignment error between segments is limited to a local portion.

5 In accordance with another aspect of the present invention, there is provided a method of manufacturing a two-dimensional phase type element, comprising the steps of: forming, on a substrate, a first etching mask in a checkered pattern; and performing an etching process while using the mask as  
10 a reference.

15 In accordance with a further aspect of the present invention, there is provided a method of manufacturing a two-dimensional phase type element, comprising the steps of: forming, on a substrate, a first etching mask in a checkered pattern; forming segments of multiple levels at a portion not covered by the first mask; forming a second etching mask corresponding to an inversion of the first etching mask; removing the first etching mask; and forming  
20 segments of multiple levels at a portion not covered by the second etching mask.

In the methods described above, the first etching mask may be formed by a chromium film.

25 The first etching mask may consist of aluminum.

The first etching mask may consist of aluminum and the second etching mask may consist of

chromium.

The first etching mask may consist of chromium and the second etching mask may consist of aluminum.

5 The substrate may contain quartz.

A reticle having an optical proximity effect correcting pattern may be used to form the etching mask of checkered pattern through photolithography.

10 The etching process may be carried out by use of the etching mask and an etching mask formed by a resist.

The method may further comprise molding an element while using, as a mold, a substrate on which plural segments of multiple levels are formed.

15 The method may be usable to produce one of a phase type computer generated hologram, a two-dimensional binary structure, and a phase modulation plate.

20 In accordance with a further aspect of the present invention, there is provided an illumination system including a two-dimensional phase type element manufactured in accordance with a method as recited above.

25 In accordance with a yet further aspect of the present invention, there is provided a projection exposure apparatus having an illumination system as recited above.

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In accordance with a still further aspect of the present invention, there is provided a device manufacturing method, comprising the steps of: exposing a wafer to a device pattern, by use of a projection exposure apparatus as recited above; and developing the exposed wafer.

These and other objects, features and advantages of the present invention will become more apparent upon a consideration of the following description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic view for explaining a resist pattern formed on a substrate in an embodiment of the present invention.

Figure 2 is a schematic view for explaining an etching depth distribution defined on a substrate in an embodiment of the present invention.

Figure 3 is a schematic view for explaining a resist pattern formed on a substrate in an embodiment of the present invention.

Figure 4 is a schematic view for explaining an etching depth distribution defined on a substrate in an embodiment of the present invention.

Figure 5 is a schematic view for explaining a

resist pattern formed on a substrate in an embodiment of the present invention.

5       Figure 6 is a schematic view for explaining an etching depth distribution defined on a substrate in an embodiment of the present invention.

      Figure 7 is a schematic view for explaining a resist pattern formed on a substrate in an embodiment of the present invention.

10       Figure 8 is a schematic view for explaining an etching depth distribution defined on a substrate in an embodiment of the present invention.

      Figure 9 is a schematic view of a substrate having an aluminum film formed thereon, in accordance with an embodiment of the present invention.

15       Figure 10 is a schematic view of a substrate having an aluminum film formed thereon and being polished by a predetermined amount.

20       Figure 11 is a schematic view for explaining a resist pattern formed on a substrate in an embodiment of the present invention.

      Figure 12 is a schematic view for explaining an etching depth distribution defined on a substrate in an embodiment of the present invention.

25       Figure 13 is a schematic view for explaining a resist pattern formed on a substrate in an embodiment of the present invention.

      Figure 14 is a schematic view for explaining

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an etching depth distribution defined on a substrate  
in an embodiment of the present invention.

Figure 15 is a schematic view for explaining  
a resist pattern formed on a substrate in an  
embodiment of the present invention.

Figure 16 is a schematic view for explaining  
an etching depth distribution defined on a substrate  
in an embodiment of the present invention.

Figure 17 is a schematic view for explaining  
invalid regions in a case where a resist pattern in an  
embodiment of the present invention is deviated.

Figure 18 is a schematic view for explaining  
invalid regions in a case where a resist pattern in an  
embodiment of the present invention is deviated.

Figures 19A - 19D are schematic views of  
reticles and resist patterns, respectively.

Figures 20A - 20D are schematic views,  
respectively, for explaining manufacture of a step-  
like diffractive optical element.

Figure 21 is a schematic view of an  
illumination system in a semiconductor exposure  
apparatus.

Figure 22 is a flow chart of semiconductor  
device manufacturing processes.

Figure 23 is a flow chart for explaining  
details of a wafer process included in the procedure  
of Figure 22.

Figures 24A - 24C are schematic view of reticles, respectively.

Figures 25A - 25C are schematic views of etching depth distributions, respectively.

Figure 26 is a sectional view of a phase type CGH.

Figure 27 is a sectional view of a phase type CGH.

Figure 28 is a schematic view for explaining invalid regions in a case where a resist pattern is deviated.

Figure 29 is a schematic view for explaining invalid regions in another case where a resist pattern is deviated.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will now be described with reference to Figures 1 - 23 of the accompanying drawings.

Referring to Figure 1, first, a chromium film 21 is formed on a quartz substrate with a thickness of about 100 nm. Then, a photoresist is applied onto the chromium film 21 and, through photolithography, a resist pattern 22 is formed thereon in a checkered pattern and with a width 1 micron, as an etching mask.

In this embodiment, quartz is used as a base material of the substrate. However, fluo~~x~~ide such as

calcium fluoride, magnesium fluoride, lithium fluoride, aluminum fluoride or the like may be used. Use of fluoride is particularly effective as a material of a phase type CGH or a phase modulation plate to be used in an exposure apparatus which uses exposure light of short wavelength such as ArF excimer laser light or F<sub>2</sub> (fluorine) excimer laser light, for example. Also, use of quartz is effective as a material of a phase type CGH or a phase modulation plate to be used in an exposure apparatus which uses ArF excimer laser light, KrF excimer laser light, or i-line light from a ultra-high pressure Hg lamp, for example. Further, the formation of the resist pattern may use any one of a stepper, an EB patterning apparatus or an ion patterning apparatus.

Figures 2, 4, 6, 8, 12 and 14 show etching depth distributions at each segment of a substrate. In the state shown in Figure 2, the etching process is not yet performed. Thus, all the etching depths of the segments of the substrate are zero (nm).

Subsequently, while using the resist pattern 22 (Figure 1) as a mask, the chromium film 21 is etched in accordance with a parallel flat plate RIE method and by using a mixture gas of chlorine and oxygen, for example, whereby a chromium film pattern is produced. The etching process may be done, in place of using the RIE method, on the basis of a

sputter etching method, an ion milling method (best suited to a case where a fluoride series material is used), a low-pressure high-density plasma method such as UHF method or an ICP method, for example.

5           Subsequently, the resist pattern 22 is peeled, by which a chromium film pattern 21a such as shown in Figure 3 is obtained. Then, a photoresist is again applied thereto, and a resist pattern 23 is formed thereon through photolithography. While the  
10       resist pattern 23 is illustrated as having circular shapes with a diameter corresponding to the length of a diagonal of the segment, it may have square shapes with a size (at each side) corresponding to the diagonal length of the segment.

15           Thereafter, while using the chromium film pattern 21a and the resist pattern 23 as a mask, the quartz substrate is etched to a depth 61 nm in accordance with the RIE method. Figure 4 shows the etching depth (nm) distribution at the segments of the  
20       quartz substrate, after the first-time etching process.

          Subsequently, the resist pattern 23 is separated and, thereafter, a photoresist is again applied to the substrate. Then, through  
25       photolithography, a resist pattern 24 such as shown in Figure 5 is formed. Although the resist pattern 24 has circular shapes similar to the resist pattern 23,

it may have square shapes with a size (at each side) corresponding to the diagonal length of the segment. Subsequently, while using the chromium film pattern 21a and the resist pattern 24 as a mask, the quartz substrate is etched to a depth 122 nm in accordance with the RIE method. Figure 6 shows the etching depth (nm) distribution at the segments of the quartz substrate, after the second-time etching process.

Then, the resist pattern 24 is separated and, thereafter, a photoresist is again applied to the substrate. Then, through photolithography, a resist pattern 25 such as shown in Figure 7 is formed. Subsequently, while using the chromium film pattern 21a and the resist pattern 25 as a mask, the substrate is etched to a depth 244 nm in accordance with the RIE method. Figure 8 shows the etching depth (nm) distribution at the segments of the quartz substrate, after the third-time etching process. While the resist pattern 25 is illustrated as having circular shapes like the resist pattern 23, it may have square shapes.

Subsequently, as shown in Figure 9, the resist pattern 25 is removed and, in accordance with a sputtering method, an aluminum film 31 with a thickness 100 nm is formed on the whole surface of the substrate. Then, the aluminum film surface is polished until the surface of the chromium pattern 21a

is exposed, by using an abrasive material of cerium oxide of a particle diameter 5/100 micron, and an abrasive cloth of urethane sheet, and with use of a lapping device, under a condition of 30 rpm and 50g/cm<sup>2</sup>.

Figure 10 is a plan view of the substrate after the polishing. As illustrated, there is produced an alternating arrangement of the chromium film pattern 21a and the aluminum film pattern 31a, wherein each of the chromium film pattern 21a group and the aluminum film pattern 31a group comprises a checkered pattern. Thereafter, the chromium film pattern 21a is removed by wet etching, while using an etching liquid based on a mixture of cerium ammonium nitrate, perchloric acid and water, for example. By removing the chromium film pattern 21a while leaving the aluminum film pattern 31a there, as described above, an aluminum film pattern (31a) having a checkered pattern corresponding to an inverse of the checkered pattern of the chromium film pattern 21a, can be produced.

Subsequently, as shown in Figure 11, a photoresist is again applied to the substrate and, through photolithography, a resist pattern 51 is formed thereon. While the resist pattern 51 is illustrated as having circular shapes with a diameter corresponding to the diagonal length of the segment,

like the resist pattern 23, it may be formed with square shapes with a size (at each side) corresponding to the diagonal length of the segment.

Then, while using the aluminum film pattern 31a and the photoresist pattern 51 as a mask, the quartz substrate is etched to a depth 61 nm, in accordance with the RIE method. Figure 12 shows the etching depth distribution at the segments of the quartz substrate, after the first-time etching.

Subsequently, the resist pattern 51 is separated and, thereafter, a photoresist is again applied to the substrate. Then, through photolithography, a resist pattern 52 such as shown in Figure 13 is formed. Thereafter, while using the aluminum film pattern 31a and the resist pattern 52 as a mask, the quartz substrate is etched to a depth 122 nm. Figure 14 shows the etching depth distribution at the segments of the quartz substrate. The resist pattern 52 may have square shapes with a size (at each side) corresponding to the diagonal length of the segment.

Subsequently, the resist pattern 52 is separated and, thereafter, a photoresist is again applied to the substrate. Then, through photolithography, a resist pattern 53 such as shown in Figure 15 is formed. Thereafter, while using the aluminum film pattern 31a and the resist pattern 53 as

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a mask, the quartz substrate is etched to a depth 244 nm. Figure 16 shows the etching depth distribution at the segments of the quartz substrate. The resist pattern 53 may have square shapes with a size (at each side) corresponding to the diagonal length of the segment.

Thereafter, the resist pattern 53 is separated and, then, the aluminum film pattern 31a is removed by wet etching, while using a mixture solvent of phosphoric acid, nitric acid, acetic acid and water, for example. By this, a phase type CGH having eight-level stepped structure (eight-level depths) is accomplished.

Figure 17 is a schematic and plane view for explaining segments in a case where, due to an alignment error, a resist pattern 23 which inherently should cover a central segment 170, is deviated in X direction by an amount corresponding to a length "d". The resist pattern 23 has a square shape with a size (at each side) of  $2^{1/2}a$ . It is inclined by 45 deg. with respect to the chromium film pattern 21a grid (square shape 21a). Zones denoted at 180 are those segments which should be etched.

Although, in Figures 3, 5 and 7, the resist pattern has a circular shape, in Figure 17 it has a square shape. This is for simplicity of explanation. Thus, the zones 61 depicted by hatching are invalid



regions. Namely, they are limited to local zones.

The area  $S_3$  thereof can be given by equation (3)

below:

$$S_3 = 2d^2 \quad \dots(3)$$

It is seen that, as compared with the example of Figure 28, as long as  $d < a$  is satisfied,  $S_1 > S_3$  applies.

Since, in the cases of ordinary patterning, the alignment can be accomplished under the condition of  $d \ll a$ , the resist pattern 23 of this embodiment can be said as narrowing the invalid region, as compared with the resist pattern 12 described hereinbefore.

Figure 18 is a schematic and plan view of segments in a case where, due to an alignment error, the resist pattern 23 which should cover a central segment is deviated in X and Y directions by an amount corresponding to a length "d", respectively. Like the case of Figure 17, the resist pattern 23 has a square shape with a size (at each side) of  $2^{1/2}a$ . It is inclined by 45 deg. with respect to the chromium film pattern 21a grid (square shape 21a). Zones denoted at 180 are those segments to be etched.

Thus, the zones 62 depicted by hatching are invalid regions. Namely, they are limited to local zones. The area  $S_4$  thereof can be given by equation (4) below:

$$S_4 = 4d^2 \quad \dots(4)$$

It is seen that, as compared with the example of

Figure 29, as long as  $d < 2a/3$  is satisfied,  $S_2 > S_4$  applies.

Since, in the cases of ordinary patterning, the alignment can be accomplished under the condition of  $d \ll a$ , the resist pattern 23 of this embodiment can be said as narrowing the invalid region, as compared with the resist pattern 12 described hereinbefore.

While the present embodiment has been compared with the conventional method in respect to two models of Figures 17 and 18, even if there occurs an alignment error in any arbitrary direction, the alignment error in the present embodiment results in a narrower invalid region.

Figure 19A is a schematic view of a reticle for forming a chromium film pattern having a checkered pattern in the present embodiment. However, a resist pattern formed by use of the reticle shown in Figure 19A may be such as shown in Figure 19B. Thus, an accurate chromium film pattern may not be produced.

In consideration of it, a reticle based on optical proximity effect correction, such as shown in Figure 19C, may be used. With this reticle, a resist pattern such as shown in Figure 19D can be produced. Thus, a chromium film pattern can be produced more accurately.

A phase type CGH, a two-dimensional binary structure or a phase modulation plate may have an

anti-reflection film, as required. By using a reflective material for the substrate or, alternatively, by forming a film of reflective material on the substrate in accordance with a vapor deposition method, a plating method, a sputtering method or a CVD method, for example, a reflective phase type CGH or a reflection type two-dimensional binary structure or a reflection type phase modulation plate can be produced. Also, a reflection reinforcing film may be formed on the surface of a reflection type element.

Figures 20A - 20D are schematic views, respectively, for explaining the procedure for manufacturing a step-like diffractive optical element.

It is seen from these drawings that a phase type CGH having been manufactured in accordance with the embodiment described above, can be used as a mold in production of a resin-made step-like diffractive optical element. More specifically, first, as shown in Figure 20A, by using a cylinder 72, drops of a resin material 73 such as a reaction-setting type resin, that is, a ultraviolet-ray setting type resin or a thermosetting type resin, of acrylic series or epoxy series, are put on a glass substrate 71.

Then, as shown in Figure 20B, a phase type CGH 74 having been manufactured in accordance with the method of the present embodiment is pressed against

the top face of the resin 73 from the above. By this, a replica layer 75 such as shown in Figure 20C is produced. Here, before pressing the mold (phase type CGH 74) against the resin 73, the surface of the CGH 74 may be coated with a mold releasing agent, as required, to facilitate the mold releasing.

Subsequently, where a ultraviolet-ray setting type resin is used, ultraviolet rays are projected to the resin 73 from the the glass substrate 71 (mold) side to cause setting of the resin 73. Where a thermosetting type resin is used, a heating treatment is carried out to cause setting of the resin 73. Thereafter, the replica layer 75 is separated from the glass substrate 71, whereby a step-like diffractive optical element 76 such as shown in Figure 20D is accomplished.

Figure 21 is a schematic view of an illumination system of a semiconductor exposure apparatus for use with exposure light of ultraviolet rays, such as i-line light or KrF excimer laser light, for example, wherein a phase type CGH having been manufactured in accordance with this embodiment is incorporated therein. The light emitted from a light source 81 goes through a beam shaping optical system 82 and impinges on a phase type CGH 83. The light passing through the CGH element 83 goes through a relay lens system 84, a stop 85, a zooming optical

system 86, a multiple-beam producing optical system 87, and a projecting means 88, and it is projected on a reticle 89. The reticle 89 has a circuit pattern formed thereon, and the reticle pattern is then projected onto a wafer by means of a projection optical system (not shown).

The phase type CGH 83 has a function for producing light of ring-like shape or quadruple shape at the position of the stop 85. Thus, by using a phase type CGH as manufactured in accordance with the method described hereinbefore, the optical performance as well as the light utilization efficiency in the modified illumination such as ring-like illumination or quadruple illumination, can be improved significantly. Further, where a semiconductor exposure apparatus to be used with ultraviolet exposure light such as i-line light or KrF excimer laser light, for example, is manufactured by using such illumination system, a high-performance semiconductor exposure apparatus can be provided.

Figure 22 is a flow chart of procedure for manufacture of semiconductor devices such as semiconductor chips (e.g. ICs or LSIs), liquid crystal panels, or CCDs, for example.

Step S1 is a design process for designing a circuit of a semiconductor device. Step S2 is a process for making a mask on the basis of the circuit

pattern design, by using an EB patterning apparatus,  
for example. Step S3 is a process for preparing a  
wafer by using a material such as silicon. Step S4 is  
a wafer process (called a pre-process) using the so  
5 prepared mask and wafer. The mask is loaded into the  
exposure apparatus described above, and the mask is  
conveyed onto a mask chuck, by which the mask is  
chucked. Then, the wafer is loaded and any alignment  
deviation is detected. The wafer stage is driven to  
10 perform the alignment. As the alignment is  
accomplished, the exposure process is carried out.  
After completion of the exposure, the wafer is moved  
stepwise to a next shot position, whereby circuits are  
practically formed on the wafer through lithography.  
15 Step S5 subsequent to this is an assembling step  
(called a post-process) wherein the wafer having been  
processed by step S4 is formed into semiconductor  
chips. This step includes an assembling (dicing and  
bonding) process and a packaging (chip sealing)  
20 process. Step S6 is an inspection step wherein  
operation check, durability check and so on for the  
semiconductor devices provided by step S5, are carried  
out. With these processes, semiconductor devices are  
completed and they are shipped (step S7).

25 Figure 23 is a flow chart showing details of  
the wafer process (step S4).

Step S11 is an oxidation process for

oxidizing the surface of a wafer. Step S12 is a CVD process for forming an insulating film on the wafer surface. Step S13 is an electrode forming process for forming electrodes upon the wafer by vapor deposition. 5 Step S14 is an ion implanting process for implanting ions to the wafer. Step S15 is a resist process for applying a resist (photosensitive material) to the wafer. Step S16 is an exposure process for printing, by exposure, the circuit pattern of the mask on the 10 wafer through the exposure apparatus described above.

Step S17 is a developing process for developing the exposed wafer. Step S18 is an etching process for removing portions other than the developed resist image. Step S19 is a resist separation process 15 for separating the resist material remaining on the wafer after being subjected to the etching process. By repeating these processes, circuit patterns are superposedly formed on the wafer.

With these processes, high density 20 microdevices can be manufactured.

As described hereinbefore, in accordance with the method of manufacturing a two-dimensional phase type element, a resist pattern (as a second etching mask to be used in combination with a first etching 25 mask of checkered pattern) is formed with a circular shape having a diameter corresponding to a diagonal length of a segment or a square shape having a size

(at each side) corresponding to the diagonal length of the segment. This enables that an alignment error is limited to a local portion. As a result, a phase type CGH, a two-dimensional binary structure or a phase modulation plate can be produced more accurately as compared with the conventional method, such that the optical performance of the element can be improved.

While the invention has been described with reference to the structures disclosed herein, it is not confined to the details set forth and this application is intended to cover such modifications or changes as may come within the purposes of the improvements or the scope of the following claims.



WHAT IS CLAIMED IS:

1. A two-dimensional phase type element having plural segments, wherein an alignment error between segments is limited to a local portion.

2. A method of manufacturing a two-dimensional phase type element, comprising the steps of:  
forming, on a substrate, a first etching mask in a checkered pattern; and  
performing an etching process while using the mask as a reference.

3. A method of manufacturing a two-dimensional phase type element, comprising the steps of:  
forming, on a substrate, a first etching mask in a checkered pattern;  
forming segments of multiple levels at a portion not covered by the first mask;  
forming a second etching mask corresponding to an inversion of the first etching mask;  
removing the first etching mask; and  
forming segments of multiple levels at a portion not covered by the second etching mask.

4. A method according to Claim 2 or 3, wherein the first etching mask is formed by a chromium film.

5. A method according to Claim 2 or 3, wherein the first etching mask consists of aluminum.

6. A method according to Claim 2 or 3, wherein the first etching mask consists of aluminum and wherein the second etching mask consists of chromium.

7. A method according to Claim 2 or 3, wherein the first etching mask consists of chromium and wherein the second etching mask consists of aluminum.

8. A method according to any one of Claims 2 - 7, wherein the substrate contains quartz.

9. A method according to any one of Claims 2 - 8, wherein a reticle having an optical proximity effect correcting pattern is used to form the etching mask of checkered pattern through photolithography.

10. A method according to any one of Claims 2 - 9, wherein the etching process is carried out by use of the etching mask and an etching mask formed by a resist.

11. A method according to any one of Claims 2 - 10, further comprising molding an element while using, as a mold, a substrate on which plural segments of

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developing the exposed wafer.

ABSTRACT OF THE DISCLOSURE

Disclosed is a method of manufacturing a two-dimensional phase type element, which includes the steps of forming, on a substrate, a first etching mask in a checkered pattern, forming segments of multiple levels at a portion not covered by the first mask, forming a second etching mask corresponding to an inversion of the first etching mask, removing the first etching mask, and forming segments of multiple levels at a portion not covered by the second etching mask.

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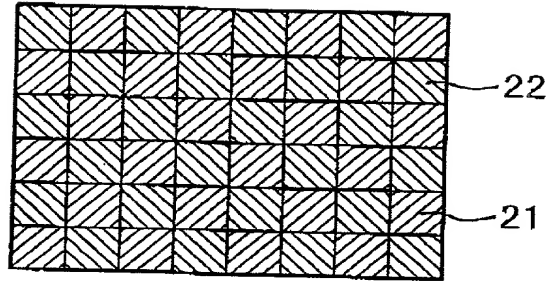


FIG. 1

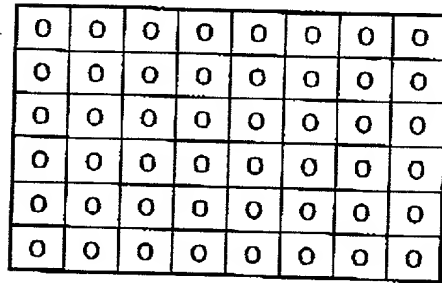


FIG. 2

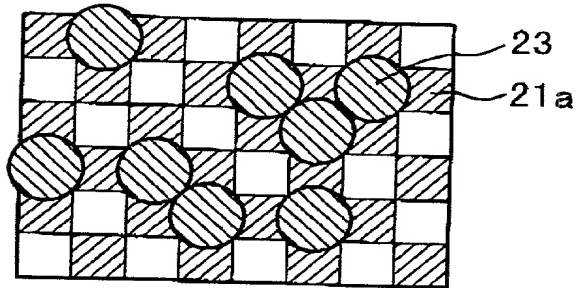


FIG. 3

0	61	0	61	0	61	0	61
61	0	61	0	0	0	0	0
0	0	0	61	0	61	0	61
0	0	61	0	0	0	61	0
0	61	0	61	0	0	0	61
61	0	0	0	61	0	61	0

FIG. 4

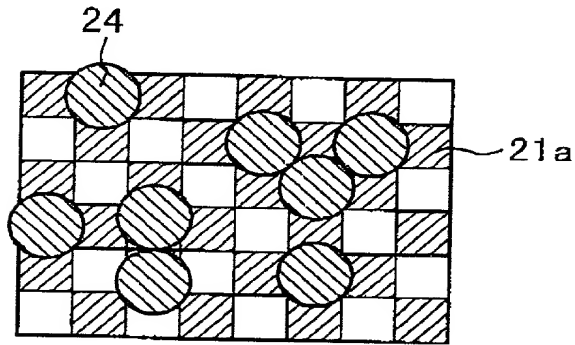


FIG. 5

0	61	0	183	0	183	0	183
183	0	183	0	0	0	0	0
0	122	0	183	0	61	0	183
0	0	61	0	122	0	122	0
0	183	0	61	0	0	0	183
122	0	122	0	183	0	183	0

FIG. 6

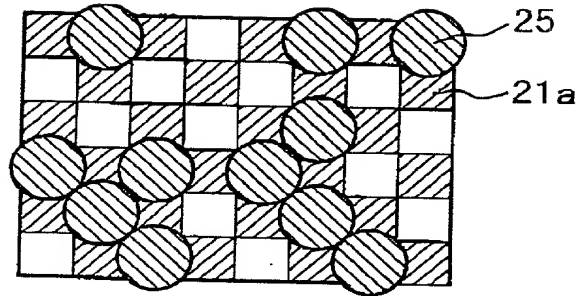


FIG. 7

0	61	0	427	0	183	0	183
427	0	427	0	244	0	244	0
0	366	0	427	0	61	0	427
0	0	61	0	122	0	305	0
0	183	0	305	0	0	0	427
366	0	122	0	427	0	183	0

FIG. 8

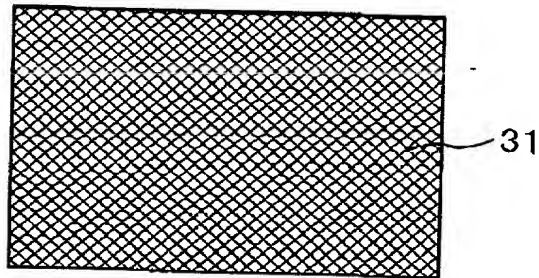


FIG. 9

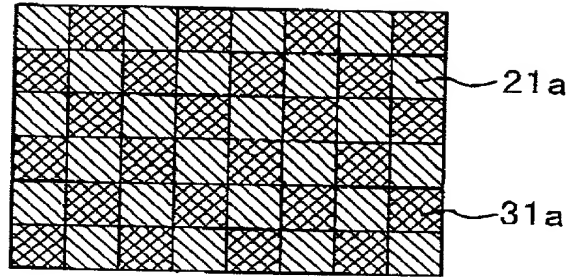


FIG. 10

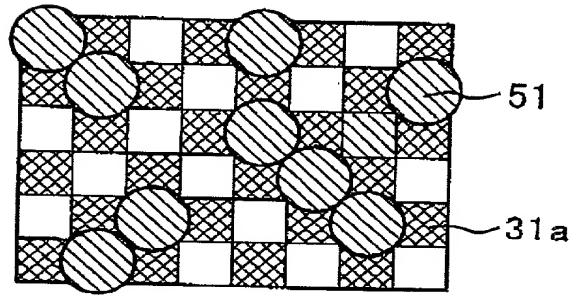


FIG. 11

0	61	61	427	0	183	61	183
427	0	427	61	244	61	244	0
61	366	61	427	0	61	61	427
0	61	61	61	122	0	305	61
61	183	0	305	61	0	0	427
366	0	122	61	427	0	183	0

FIG. 12



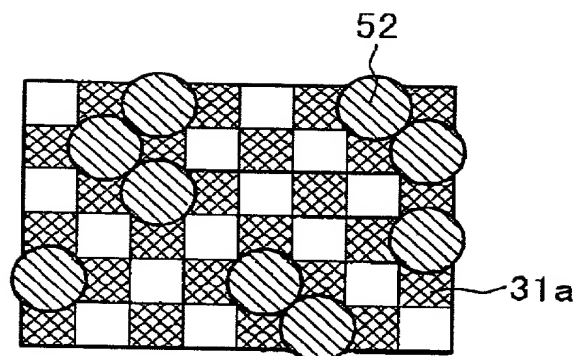


FIG. 13

122	61	61	427	122	183	61	183
427	0	427	183	244	183	244	0
183	366	61	427	122	61	183	427
0	61	61	183	122	122	305	61
61	183	122	305	183	0	122	427
366	122	122	183	427	0	183	0

FIG. 14

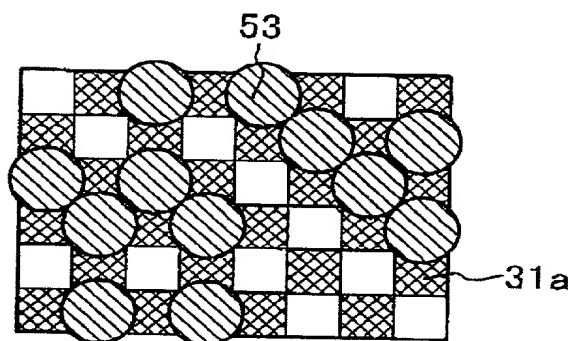


FIG. 15

366	61	61	427	122	183	305	183
427	244	427	427	244	183	244	0
183	366	61	427	366	61	183	427
0	183	61	183	122	366	305	61
305	183	366	305	427	0	366	427
366	122	122	183	427	244	183	366

FIG. 16

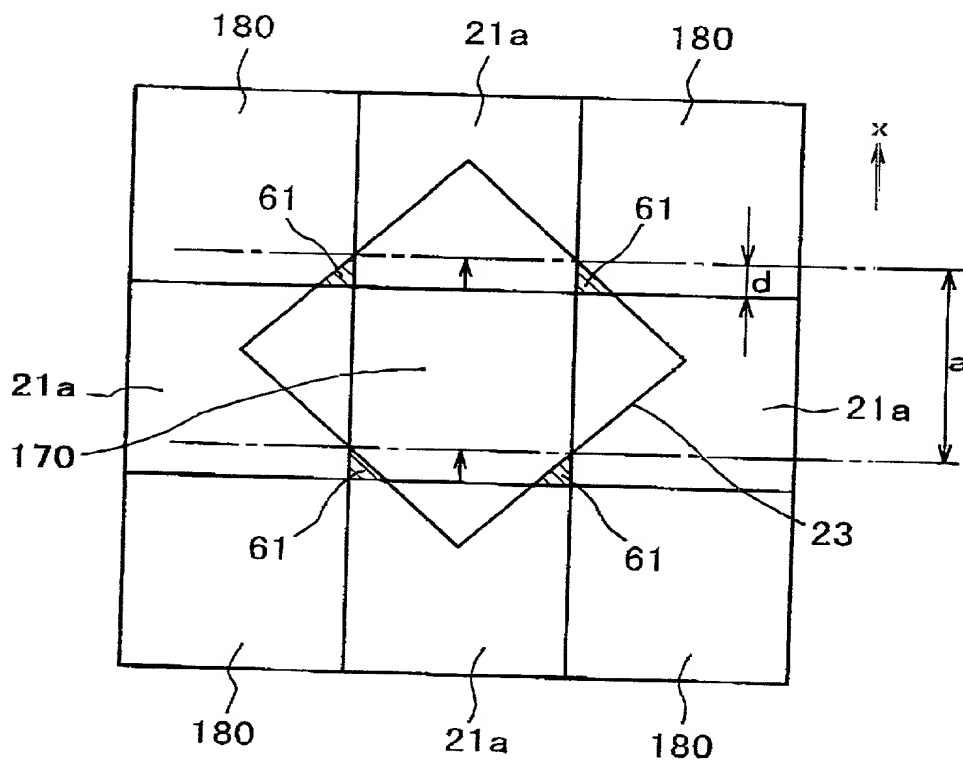
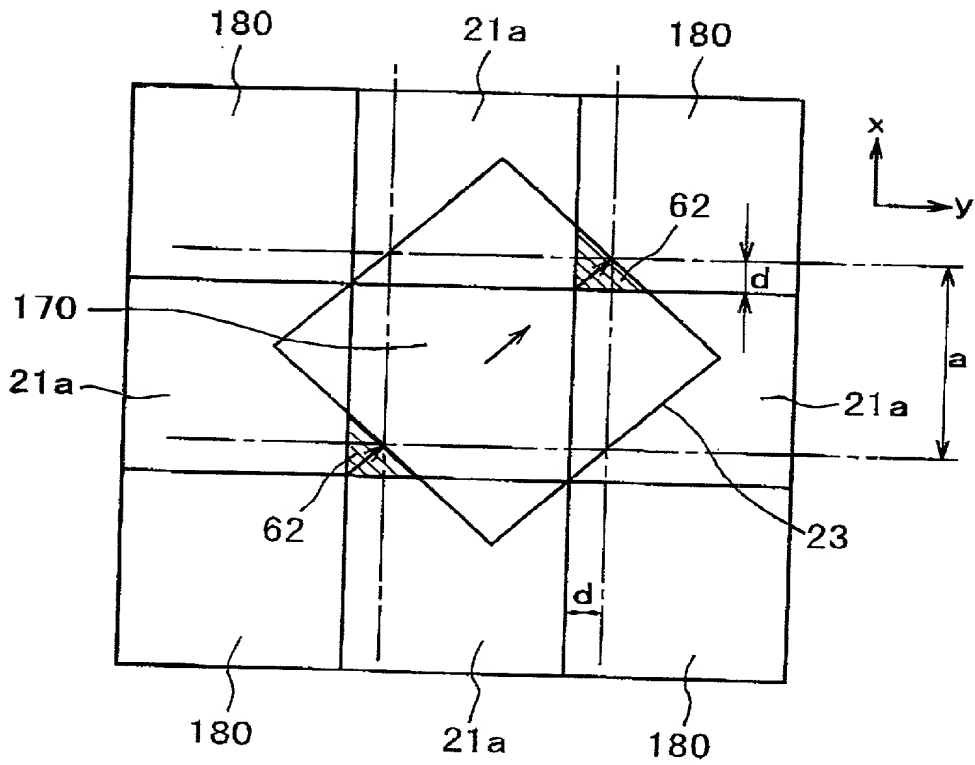
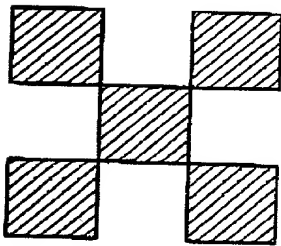


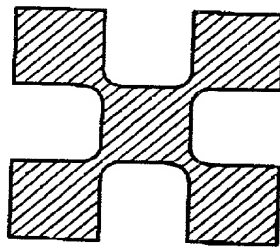
FIG. 17



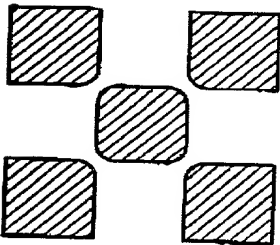
**FIG. 18**



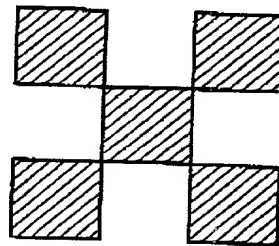
**FIG. 19A**



**FIG. 19B**



**FIG. 19C**



**FIG. 19D**

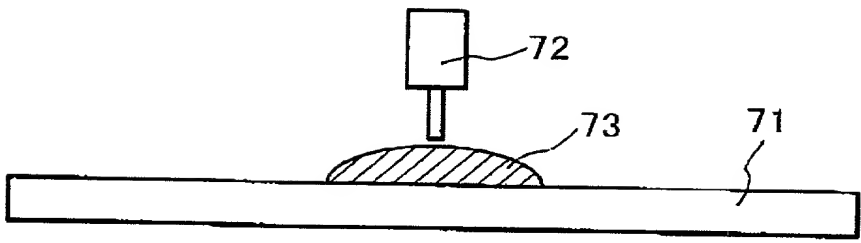


FIG. 20A

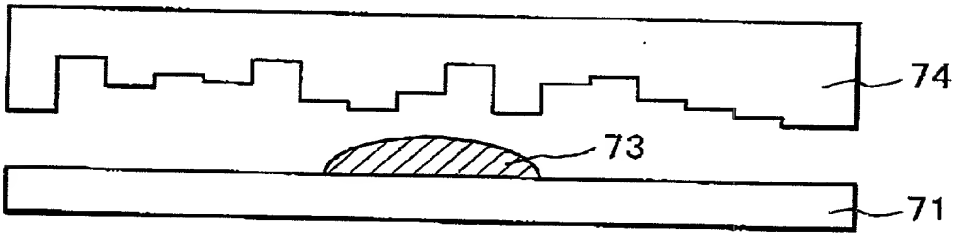


FIG. 20B

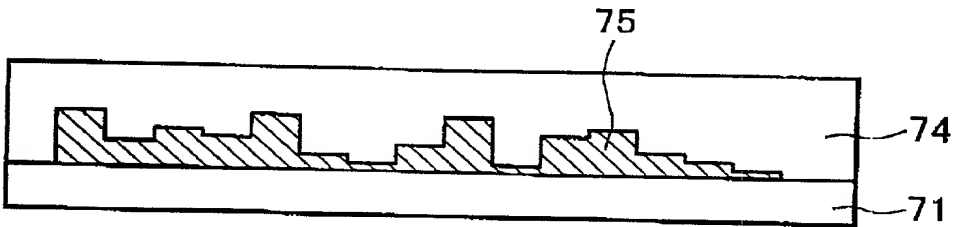


FIG. 20C

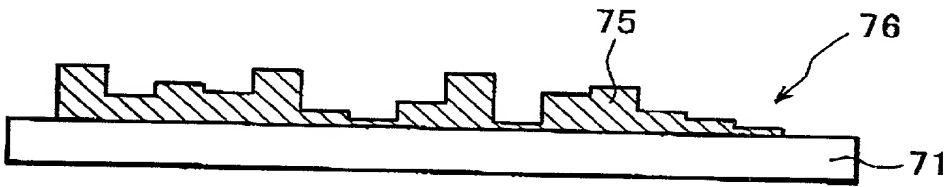


FIG. 20D

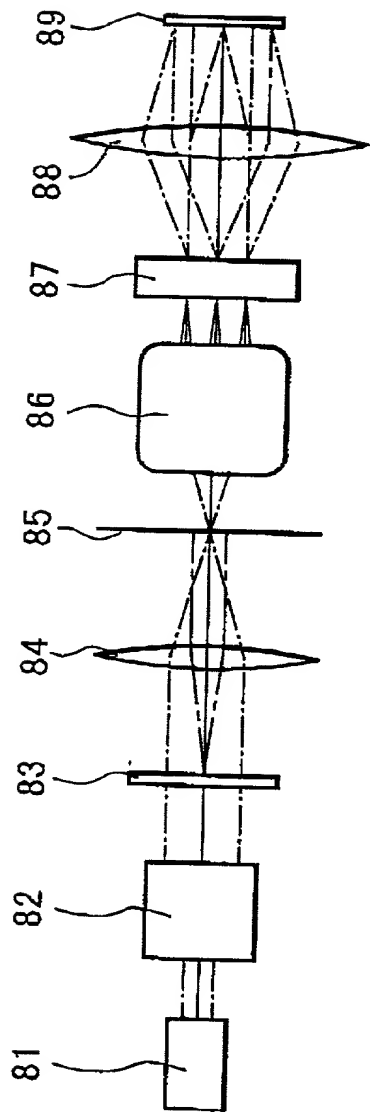


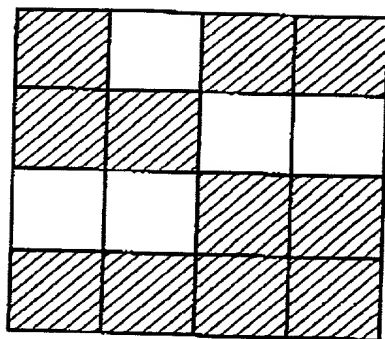
FIG. 21

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graph TD
    A[CIRCUIT DESIGNN] -- "(STEP S1)" --> B[MASK MANUFACTURE]
    B -- "(STEP S2)" --> C[WAFER PROCESS  
(PRE-PROCESS)]
    D[WAFER MANUFACTURE] -- "(STEP S3)" --> C
    C -- "(STEP S4)" --> E[ASSEMBLY PROCESS  
(POST-PROCESS)]
    E -- "(STEP S5)" --> F[INSPECTION]
    F -- "(STEP S6)" --> G[SHIPMENT]
    G -- "(STEP S7)" --> H[ ]
  
```

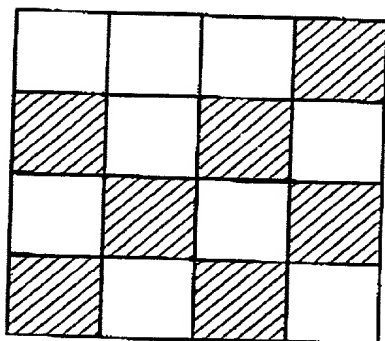
FIG. 22

FIG. 23



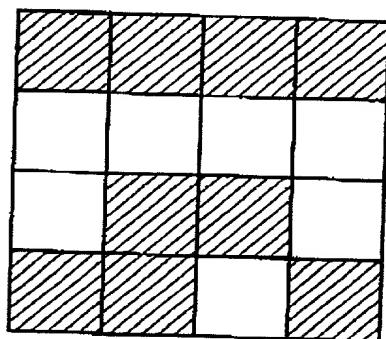
← 1a

**FIG. 24A**



← 1b

**FIG. 24B**



← 1c

**FIG. 24C**



0	61	0	0
0	0	61	61
61	61	0	0
0	0	0	61

**FIG. 25A**

122	183	122	0
0	122	61	183
183	61	122	0
0	122	0	183

**FIG. 25B**

122	183	122	0
244	366	305	427
427	61	122	244
0	122	244	183

**FIG. 25C**

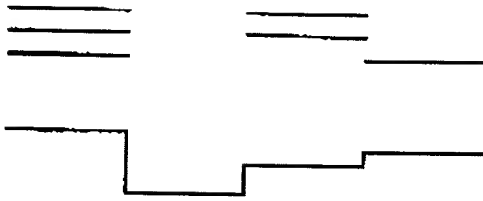


FIG. 26

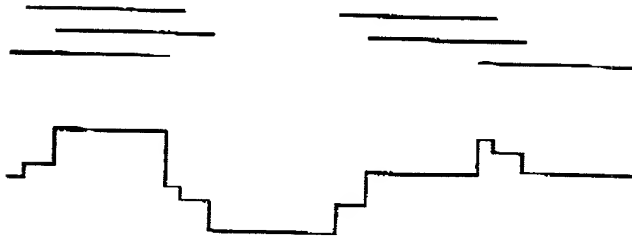


FIG. 27

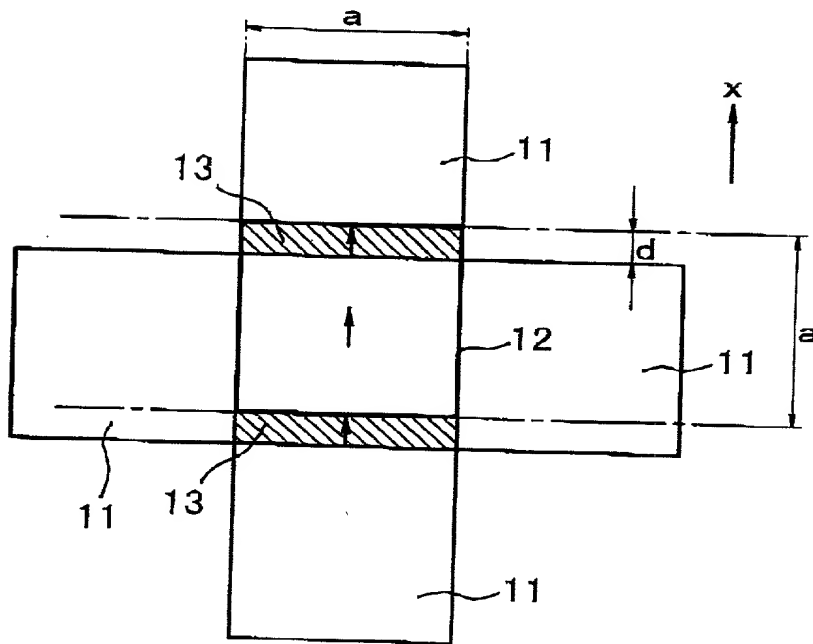


FIG. 28

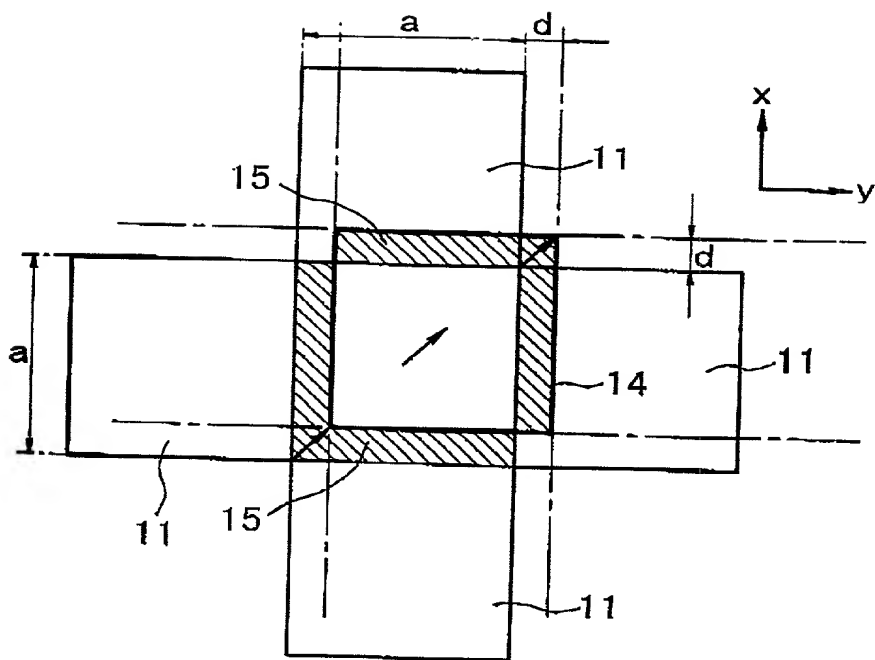


FIG. 29